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EXAMINER	
O#BRIEN, BARRY J	

ART UNIT	PAPER NUMBER
2183	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/903,208	TOPHAM, NIGEL PETER	
	Examiner	Art Unit	
	Barry J. O'Brien	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 June 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) *16-29* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2 and 4*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-15 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed on record in the file: Response to Restriction Requirement as received on 6/21/04.

Election/Restrictions

3. Applicant's election without traverse of Group I, claims 1-15, in the reply filed on 6/21/04 is acknowledged.

Specification

4. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

5. The applicant is requested to review the specification and update the status of all co-pending applications made mention of, replacing attorney docket numbers with current U.S. application or patent numbers when appropriate.

6. The title of the invention is not descriptive. The present title is very generic, relating only to the broad field of the invention and not more clearly stating what the invention as claimed is directed towards. A new title is required that is clearly indicative of the invention to which the claims are directed.

7. The abstract of the disclosure is objected to because it contains the label "[Fig. 3(B)]" at the end of the abstract. It is unclear why this label is on the abstract, and the Examiner assumes that it was a typographical error. Further, as noted above, the abstract refers to the purported merits of the invention in the last paragraph of the abstract. Correction is required. See MPEP § 608.01(b).

8. Applicant is reminded of the proper content of an abstract of the disclosure.

A patent abstract is a concise statement of the technical disclosure of the patent and should include that which is new in the art to which the invention pertains. If the patent is of a basic nature, the entire technical disclosure may be new in the art, and the abstract should be directed to the entire disclosure. If the patent is in the nature of an improvement in an old apparatus, process, product, or composition, the abstract should include the technical disclosure of the improvement. In certain patents, particularly those for compounds and compositions, wherein the process for making and/or the use thereof are not obvious, the abstract should set forth a process for making and/or use thereof. If the new technical disclosure involves modifications or alternatives, the abstract should mention by way of example the preferred modification or alternative.

The abstract should not refer to purported merits or speculative applications of the invention and should not compare the invention with the prior art.

Where applicable, the abstract should include the following:
(1) if a machine or apparatus, its organization and operation;
(2) if an article, its method of making;
(3) if a chemical compound, its identity and use;
(4) if a mixture, its ingredients;
(5) if a process, the steps.

Extensive mechanical and design details of apparatus should not be given.

Claim Rejections - 35 USC § 101

9. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

10. Claims 1-15 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

11. Claim 1 is directed towards a processor with "internal" and "external" instruction formats without being tangibly embodied on some sort of computer-readable medium. Thus the claim language is attempting to claim the "processor instruction encodings" as either a data structure, or a program without a machine to execute the program on, both of which are considered to be non-statutory subject matter. Dependent claims 2-13 contain all the limitations of their parent claims, and thus are rejected for the same reasons as claim 1.

12. Claim 14 is directed towards "Processor instruction encodings" without being tangibly embodied on some sort of computer-readable medium. Thus the claim language is attempting to claim the "processor instruction encodings" as either a data structure, or a program without a machine to execute the program on, both of which are considered to be non-statutory subject matter.

13. Claim 15 is directed towards, "A method of encoding processor instructions for a processor" without being tangibly embodied on some sort of computer-readable medium. Thus the claim language is attempting to claim a method for use in a processor without the processor actually performing any steps, making it a non-computer implemented method, which is considered to be non-statutory subject matter.

Claim Rejections - 35 USC § 112

14. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it

> pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

15. Claim 1 is rejected under 35 U.S.C. 112, first paragraph. Specifically, since the claimed invention is not supported by either a specific and substantial asserted utility or a well established utility for the reasons set forth above, one skilled in the art clearly would not know how to use the claimed invention. Here, the claim language is directed towards a data structure, specifically a processor with "internal" and "external" instruction formats, without being tangibly embodied on some sort of computer-readable medium (see corresponding 35 U.S.C. 101 rejection above). A data structure by itself has no utility without something to act upon the data, such as a computer-implemented method, and thus claim 1 lacks utility. Dependent claims 2-13 contain all of the limitations of their parent claims, and thus are rejected for the same reasons as claim 1.

16. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

17. Claims 1-13 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

18. Claim 1 recites the limitation "the operations" in lines 11-12. There is insufficient antecedent basis for this limitation in the claim. Further, it is unclear if "the operations" refer to the "an operation" claimed in line 5, or whether the plurality of operations refers to the "first and second internal instruction formats", or they refer to two separate operations defined by "each instruction having an opcode", or something else altogether. Dependent claims 2-13 contain all the limitations of their parent claims, and thus are rejected for the same reasons as claim 1.

19. Claim 3 recites the limitation, "respective first and second internal instruction formats" on its eighth and ninth lines. It is unclear what these two "internal instruction formats" are "respective" to, and the limitations inclusion in the claim language seems unnecessary. Please correct the claim language to more clearly define any potential relationships to these "instruction formats" as well as to more clearly define the metes and bounds of the invention as claimed.

20. Claim 4 recites the limitation, "the two external formats" on lines 12-13 of the claim, and again on lines 16-17. It is unclear which two external formats this limitation refers to, as "first", "second" and "third" external formats have been defined in claim 4 and its parent claim 3. Please correct the claim language to more clearly define the metes and bounds of the invention as claimed.

21. Claim 9 recites the limitations, "one external format" and "another external format" on its second and third lines. There is insufficient antecedent basis for these limitations in the claims. Further, it is unclear if the "one" and "another" external formats are to refer to the "first" and "second" external formats in some manner as defined in parent claim 1. Please correct the claim language to more clearly define the metes and bounds of the invention as claimed.

Claim Rejections - 35 USC § 102

22. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

23. Claims 1-4 and 9-15 are rejected under 35 U.S.C. 102(b) as being anticipated by Kissell, *MIPS16: High-Density MIPS for the Embedded Market.*

24. Regarding claims 1, 14 and 15, taking claim 1 as exemplary, Kissell has taught a processor having:

a. Respective first and second external instruction formats (see MIPS16 and MIPS, respectively, see p.4 lines 24-32) in which instructions are received by the processor, each instruction having an opcode which specifies an operation to be executed (see p.5 lines 10-13), and each external format having one or more preselected opcode bits in which the opcode appears (see Opcode of MIPS16 and MIPS-I instructions in Fig.4),

b. An internal instruction format into which instructions in the external formats are translated prior to execution of the operations (see Fig.3 and p.4 lines 29-35). Here, the internal pipeline executes instructions in the standard MIPS architecture, with MIPS16 instructions being translated (decompressed) into MIPS instructions, and 32-bit MIPS instructions are translated using a "null translation" into MIPS instructions for execution in the pipeline.

c. Wherein the operations comprise a first operation specifiable in both said first and second external formats (see p.4 lines 30-32), and a second operation specifiable in said second external format (see Fig.4 and p.5 lines 10-13). Here, any MIPS16 operation is specifiable in both MIPS16 format and MIPS format. However, certain MIPS operations (i.e. those that use longer opcodes, a register that is un-specifiable in MIPS16 instruction format (due to one bit fewer in its source/target

register fields), those that use longer immediate values, or those that require 64-bit data words) cannot be specified in the MIPS instruction format.

d. Said first and second operations have distinct opcodes in said second external format (see Fig.4 and p.5 lines 10-13). Here, because any MIPS16 operation can be specified in the MIPS instruction format, but not all MIPS operations can be specified in MIPS16, any first operation that is specifiable by MIPS16 and MIPS (and can be directly translated as in Fig.4) inherently has a different opcode than an instruction not specifiable in MIPS16, otherwise the two operations would be identical.

e. In each said preselected opcode bit which the first and second external formats have in common, the opcodes of the first operation in the two external formats are identical (see Fig.4, p.4 lines 30-32 and p.5 lines 10-13). Here, the definition of the opcode mapping between MIPS-I and MIPS16 instructions (as shown in Fig.4) is that a pre-selected portion of the opcodes in both instruction formats are defined to have identical bits (see the opcodes of Load Byte instruction in *Product Description: MIPS Application-Specific Extension*, p.26, cited as showing the definition of the opcodes and as authorized by the MPEP § 2131.01(II)).

25. Claims 14 and 15 are nearly identical to claim 1. Claim 14 differs in that it is comprised as processor instruction encodings, but its limitations encompass the same scope as claim 1. Claim 15 differs in that it is comprised as a method for encoding processor instructions, but its limitations also encompass the same scope as claim 1. Therefore, claims 14 and 15 are rejected for the same reasons as claim 1.

26. Regarding claim 2, Kissell has taught a processor as claimed in claim 1, wherein:

a. The operations comprise one or more further first operations, each specifiable in both said first and second external formats, and one or more further second operations specifiable in said second external format (see Fig.4, p.4 lines 24-32, and p.5 lines 10-13). Here, any MIPS16 operation is specifiable in both MIPS16 format and MIPS format. However, not every MIPS operation can be specified in the MIPS instruction format. Further, there are multiple MIPS16 operations that can be specified in MIPS and MIPS16, as well as multiple MIPS operations that are only specifiable in MIPS.

b. For every pair of operations, made up of one said first operation and one said second operation, the operations of the pair have distinct opcodes in said second external format (see Fig.4 and p.5 lines 10-13). Here, because any MIPS16 operation can be specified in the MIPS instruction format, but not all MIPS operations can be specified in MIPS16, any first operation that is specifiable by MIPS16 and MIPS (and can be directly translated as in Fig.4) inherently has a different opcode than an instruction not specifiable in MIPS16, otherwise the two operations would be identical.

c. In each said preselected opcode bit which the first and second external formats have in common, the opcodes of each first operation in the two external formats are identical (see Fig.4, p.4 lines 30-32 and p.5 lines 10-13). Here, the definition of the opcode mapping between MIPS-I and MIPS16 instructions (as shown in Fig.4) is that a pre-selected portion of the opcodes in both instruction formats are

defined to have identical bits (see the opcodes of Load Byte instruction in *Product Description: MIPS Application-Specific Extension*, p.26, cited as showing the definition of the opcodes and as authorized by the MPEP § 2131.01(II)).

27. Regarding claim 3, Kissell has taught a processor as claimed in claim 1, having:

a. A third external instruction format (MIPS-III) in which instructions are received by the processor (see p.4 lines 24-32 and p.5 lines 10-13), each instruction having an opcode which specifies an operation to be executed (see p.5 lines 10-13), and said third external format having one or more preselected opcode bits in which the opcode appears (see "major opcode" of MIPS-III instructions on p.5 lines 10-13).

b. Respective first and second internal instruction formats into which instructions in the external formats are translated prior to execution of the operations (see Fig.3 and p.4 lines 29-35). Here, the first internal format is considered to be what MIPS16 instructions are translated in, namely MIPS instructions using the MIPS16 Decompression Block (see Fig.3), and the second internal format is considered to be what MIPS-III instructions are translated into, also MIPS instructions, but using a "null translation".

c. Wherein said second operations is specifiable in both said second and third external formats (see p.4 lines 24-32). Here, any MIPS16 operation is specifiable in MIPS16 instruction format, MIPS-I/II instruction format, and MIPS-III instruction format.

d. An instruction specifying said first operation in either said first or second external format is translated into said first internal format, an and instruction specifying

said second operation in either said second or third external format is translated into said second internal format (see Fig.3 and p.4 lines 29-35). Here, the first internal format is considered to be what MIPS16 instructions are translated in, namely MIPS instructions using the MIPS16 Decompression Block (see Fig.3), and the second internal format is considered to be what MIPS-III instructions are translated into, also MIPS instructions, but using a "null translation". Because a first operation (MIPS16) can be specified in MIPS16 or MIPS-I/II or MIPS-III formats, and a second operation (MIPS-I/II or MIPS-III) can be specified only in MIPS-I/II or MIPS-III formats, the first operation is translated into the format MIPS16 are translated into, and the second operation into the same format, although it is considered to be the format that MIPS-III instructions are translated into.

e. In each said preselected opcode bit which the second and third external formats have in common, the opcodes of the second operation in the two external formats are identical (see Fig.4, p.4 lines 30-32 and p.5 lines 10-13). Here, the definition of the opcode mapping between MIPS-I and MIPS16 instructions (as shown in Fig.4) is that a pre-selected portion of the opcodes in both instruction formats are defined to have identical bits (see the opcodes of Load Byte instruction in *Product Description: MIPS Application-Specific Extension*, p.26, cited as showing the definition of the opcodes and as authorized by the MPEP § 2131.01(II)). Because MIPS-III instructions are directly translatable and 100% fully compatible with MIPS-I instructions (see Col.4 lines 24-32 and Col.5 lines 10-13), the opcode bits

that MIPS-I/II instructions have in common with MIPS-III instructions are inherently identical as well.

28. Regarding claim 4, Kissell has taught a processor as claimed in claim 3, wherein:

a. The operations comprise one or more further first operations, each specifiable in both said first and second external formats, and one or more further second operations specifiable in said second external format (see Fig.4, p.4 lines 24-32, and p.5 lines 10-13). Here, any MIPS16 operation is specifiable in both MIPS16 format and MIPS format. However, not every MIPS operation can be specified in the MIPS instruction format. Further, there are multiple MIPS16 operations that can be specified in MIPS and MIPS16, as well as multiple MIPS operations that are only specifiable in MIPS. (DONE)

b. For every pair of operations, made up of one said first operation and one said second operation, the operations of the pair have distinct opcodes in said second external format (see Fig.4 and p.5 lines 10-13). Here, because any MIPS16 operation can be specified in the MIPS instruction format, but not all MIPS operations can be specified in MIPS16, any first operation that is specifiable by MIPS16 and MIPS (and can be directly translated as in Fig.4) inherently has a different opcode than an instruction not specifiable in MIPS16, otherwise the two operations would be identical. (DONE)

c. In each said preselected opcode bit which the first and second external formats have in common, the opcodes of each first operation in the two external formats are identical (see Fig.4, p.4 lines 30-32 and p.5 lines 10-13). Here, the definition

of the opcode mapping between MIPS-I and MIPS16 instructions (as shown in Fig.4) is that a pre-selected portion of the opcodes in both instruction formats are defined to have identical bits (see the opcodes of Load Byte instruction in *Product Description: MIPS Application-Specific Extension*, p.26, cited as showing the definition of the opcodes and as authorized by the MPEP § 2131.01(II)). (DONE)

d. In each said preselected opcode bit which the second and third external formats have in common, the opcodes of each first operation in the two external formats are identical (see Fig.4, p.4 lines 30-32 and p.5 lines 10-13). Here, the definition of the opcode mapping between MIPS-I and MIPS16 instructions (as shown in Fig.4) is that a pre-selected portion of the opcodes in both instruction formats are defined to have identical bits (see the opcodes of Load Byte instruction in *Product Description: MIPS Application-Specific Extension*, p.26, cited as showing the definition of the opcodes and as authorized by the MPEP § 2131.01(II)). Because MIPS-III instructions are directly translatable and 100% fully compatible with MIPS-I instructions (see Col.4 lines 24-32 and Col.5 lines 10-13), the opcode bits that MIPS-I/II instructions have in common with MIPS-III instructions are inherently identical as well.

29. Regarding claim 9, Kissell has taught a processor as claimed in claim 1, wherein one external format has an instruction width different from that of another external format (see MIPS16 and MIPS, respectively, in Fig.4 and p.4 lines 24-29).

30. Regarding claim 10, Kissell has taught a processor as claimed in claim 1, having:

a. A translation unit (see MIPS16 Decompression Block in Fig.3) which performs a predetermined translation operation to translate each said external-format opcode into a corresponding internal-format opcode (see Fig.3 and p.4 lines 29-35). Here, the internal pipeline executes instructions in the standard MIPS architecture, with MIPS16 instructions being translated (decompressed) into MIPS instructions, and 32-bit MIPS instructions are translated using a "null translation" into MIPS instructions for execution in the pipeline.

31. Regarding claim 11, Kissell has taught a processor as claimed in claim 10, wherein said translation operation involves selecting and/or permuting bits amongst said preselected opcode bits in the external-format instruction (see Fig.4 and p.5 line 2 – p.6 line 2). Here, opcode bits of the MIPS16 instructions are selected and mapped into the internal MIPS instruction format during translation.

32. Regarding claim 12, Kissell has taught a processor as claimed in claim 10, wherein the translation operation is independent of the external-format opcode (see Fig.4 and p.5 lines 10-13). Here, the translation is performed using a mapping, and thus is independent of the opcode value.

33. Regarding claim 13, Kissell has taught a processor as claimed in claim 12, wherein the translation unit identifies the internal format into which each external-format instruction is to be translated, and carries out said translation operation according to the identified internal format (see Figs.3-4, p.4 lines 30-33 and p.5 lines 10-13). Here, the MIPS16 Decompression Block identifies MIPS as the target internal format and translates MIPS16 instructions into MIPS

instructions. Instructions that are already in uncompressed (MIPS) format can then be considered to use a "null translation" to be put into the internal format.

34. Regarding claim 14, Kissell has taught processor instruction encodings having:

a. Respective first and second external instruction formats (see MIPS16 and MIPS, respectively, see p.4 lines 24-32) in which the instructions are received by a processor, each instruction having an opcode which specifies an operation to be executed (see p.5 lines 10-13), and each external format having one or more preselected opcode bits in which the opcode appears (see Opcode of MIPS16 and MIPS-I instructions in Fig.4),

b. An internal instruction format into which the processor instructions in the external formats are translated prior to execution of those operations (see Fig.3 and p.4 lines 29-35). Here, the internal pipeline executes instructions in the standard MIPS architecture, with MIPS16 instructions being translated (decompressed) into MIPS instructions, and 32-bit MIPS instructions are translated using a "null translation" into MIPS instructions for execution in the pipeline.

c. Wherein a first operation executable by the processor is specifiable in both said first and second external formats (see p.4 lines 30-32), and a second operation executable by the processor is specifiable in said second external format (see Fig.4 and p.5 lines 10-13). Here, any MIPS16 operation is specifiable in both MIPS16 format and MIPS format. However, certain MIPS operations (i.e. those that use longer opcodes, a register that is un-specifiable in MIPS16 instruction format (due to one bit fewer in its source/target register fields), those that use

longer immediate values, or those that require 64-bit data words) cannot be specified in the MIPS instruction format.

d. Said first and second operations have distinct opcodes in said second external format (see Fig.4 and p.5 lines 10-13). Here, because any MIPS16 operation can be specified in the MIPS instruction format, but not all MIPS operations can be specified in MIPS16, any first operation that is specifiable by MIPS16 and MIPS (and can be directly translated as in Fig.4) inherently has a different opcode than an instruction not specifiable in MIPS16, otherwise the two operations would be identical.

e. In each said preselected opcode bit which the first and second external formats have in common, the opcodes of the first operation in the two external formats are identical (see Fig.4, p.4 lines 30-32 and p.5 lines 10-13). Here, the definition of the opcode mapping between MIPS-I and MIPS16 instructions (as shown in Fig.4) is that a pre-selected portion of the opcodes in both instruction formats are defined to have identical bits (see the opcodes of Load Byte instruction in *Product Description: MIPS Application-Specific Extension*, p.26, cited as showing the definition of the opcodes and as authorized by the MPEP § 2131.01(II)).

35. Regarding claim 15, Kissell has taught a method of encoding processor instructions for a processor having respective first and second external instruction formats (see MIPS16 and MIPS, respectively, see p.4 lines 24-32) in which instructions are received by the processor, each instruction having an opcode which specifies an operation to be executed (see p.5 lines 10-13), and each external format having one or more preselected opcode bits in which the opcode

appears (see Opcode of MIPS16 and MIPS-I instructions in Fig.4), the processor also having an internal instruction format into which instruction in the external formats are translated prior to execution of the operations (see Fig.3 and p.4 lines 29-35), and the operations comprise a first operation specifiable in both said first and second external formats (see p.4 lines 30-32), and a second operation specifiable in said second external format (see Fig.4 and p.5 lines 10-13), said method comprising:

a. Encoding said first and second operations with distinct opcodes in said second external format (see Fig.4 and p.5 lines 10-13). Here, because any MIPS16 operation can be specified in the MIPS instruction format, but not all MIPS operations can be specified in MIPS16, any first operation that is specifiable by MIPS16 and MIPS (and can be directly translated as in Fig.4) inherently has a different opcode than an instruction not specifiable in MIPS16, otherwise the two operations would be identical.

b. Encoding the opcodes of the first operation in said first and second external formats so that, in each said preselected opcode bit which the first and second external formats have in common, the opcodes of the first operation I the two external formats are identical (see Fig.4, p.4 lines 30-32 and p.5 lines 10-13). Here, the definition of the opcode mapping between MIPS-I and MIPS16 instructions (as shown in Fig.4) is that a pre-selected portion of the opcodes in both instruction formats are defined to have identical bits (see the opcodes of Load Byte instruction in *Product Description: MIPS Application-Specific*

Extension, p.26, cited as showing the definition of the opcodes and as authorized by the MPEP § 2131.01(II)).

Claim Rejections - 35 USC § 103

36. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

37. Claims 5-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kissell, *MIPS16: High-Density MIPS for the Embedded Market,* as applied to claim 1 above, and further in view of Lin, U.S. Patent No. 6,633,969.

38. Regarding claim 5, Kissell has taught a processor as claimed in claim 1, but has not explicitly taught wherein the processor is a VLIW processor, wherein one external format is a scalar instruction format used for scalar instructions, and another external format is a VLIW instruction format used for VLIW instructions.

39. However, Lin has taught a VLIW processor with the ability to execute instructions in both long instruction word external formats (see Figs. 4B, 4D and Col.6 lines 12-48) and a scalar external formats (see Figs. 4A, 4C and Col.6 lines 12-48), allowing a 32-bit MIPS instruction to be produced every clock cycle so that processor throughput is increased (see Col.3 lines 1-16) while reducing the amount of storage space needed for the instructions (see Col.2 lines 1-39). One of ordinary skill in the art would have recognized that it is desirable to improve processor throughput, as well as to reduce instruction storage space required by a program. Therefore, one

of ordinary skill in the art would have found it obvious to modify the processor of Kissell to use VLIW instruction formats along with scalar instruction formats so that processor throughput can be increased and required storage space decreased.

40. Regarding claim 6, Kissell has taught a processor as claimed in claim 1, but has not explicitly taught wherein the processor is a VLIW processor, wherein the external formats are or comprise two different VLIW formats.

41. However, Lin has taught a VLIW processor with the ability to execute instructions in both long instruction word external formats (see Figs. 4B, 4D and Col.6 lines 12-48) and a scalar external formats (see Figs. 4A, 4C and Col.6 lines 12-48), allowing a 32-bit MIPS instruction to be produced every clock cycle so that processor throughput is increased (see Col.3 lines 1-16) while reducing the amount of storage space needed for the instructions (see Col.2 lines 1-39). One of ordinary skill in the art would have recognized that it is desirable to improve processor throughput, as well as to reduce instruction storage space required by a program. Therefore, one of ordinary skill in the art would have found it obvious to modify the processor of Kissell to use VLIW instruction formats along with scalar instruction formats so that processor throughput can be increased and required storage space decreased.

42. Regarding claim 7, Kissell in view of Lin has taught a processor as claimed in claim 6, wherein the two different VLIW formats are used in different respective instruction slots of a VLIW instruction parcel (see Fig. 4D). Here, the long instruction word parcel (instruction data block) contains both the 16-bit MIPS16 format (see Fig. 4B) as well as the 32-bit MIPS16 format (see Fig.4C) (see Col.6 lines 35-48)

43. Regarding claim 8, Kissell in view of Lin has taught a processor as claimed in claim 6, wherein at least one instruction slot of a VLIW instruction parcel uses the two different VLIW formats (see Fig. 4D). Here, the long instruction word parcel (instruction data block) contains both the 16-bit MIPS16 format (see Fig. 4B) as well as the 32-bit MIPS16 format (see Fig.4C) (see Col.6 lines 35-48).

Conclusion

44. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

45. Jaggar, European Patent Application EP 1296225 A2, has taught a processor with the ability to execute both a 16 and a 32-bit instruction set.

46. Pechanek et al., U.S. Patent No. 6,321,322, has taught a VLIW processor which can execute instructions in a plurality of VLIW and scalar instruction formats on the same processing core.

47. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Barry J. O'Brien whose telephone number is (703) 305-5864. After October 12th, 2004, the examiner can be reached at (571) 272-4171. The examiner can normally be reached on Mon.-Fri. 6:30am-4:00pm, with the exception of first Friday of every bi-week.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached at (703) 305-9712, or at (571) 272-4162 on or after October 12th, 2004. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

48. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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